IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application No. 10/557,623

Confirmation No. 1486

Applicant: Huitema et al.

Filed: November 17, 2005

TC/AU: 2823

Examiner: William D. Coleman

Docket No.: 259341 (Client Reference No. P80369US00)

Customer No.: 23460

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO OFFICE ACTION

Sir:

In reply to the Office Action dated April 17, 2007, please enter the following amendments and consider the following remarks.

Amendments to the Title are on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Amendments to the Drawings begin on page 5 of this paper.

Remarks begin on page 6 of this paper.

AMENDMENTS TO THE TITLE

Replace the title with: "Field Effect Transistor Including An Organic Semiconductor and A Dielectric Layer Having A Substantially Same Pattern"

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Currently amended) A method of manufacturing an electronic device, in which method at least one field effect transistor is provided on a substrate, which provision of the at least one field effect transistor comprises the steps of:

applying a patterned first conductor layer on the substrate;

applying an organic semiconductor layer on the first conductor layer;

applying a dielectric layer on the organic semiconductor layer;

patterning the organic semiconductor layer and the dielectric layer together; and

applying a patterned second conductor layer on the patterned dielectric layer.

2. (Currently amended) ~~A method as claimed in~~The method of claim 1 wherein the step of patterning the organic semiconductor layer and the dielectric layer comprises removing the organic semiconductor layer and the dielectric layer from areas not associated with the at least one field effect transistor and from areas not associated with crossing conductors of the first and second conductor layer.

3. (Currently amended) ~~A method as claimed in~~The method of claim 2, wherein the said areas associated with a field effect transistor and/or the said areas associated with crossing conductors include protection zones providing a minimal lateral distance between a first conductor in the first conductor layer and a second conductor in the second conductor layer.

4. (Currently amended) ~~A method as claimed in~~The method of claim 1 wherein the step of applying an organic semiconductor layer on the first conductor layer comprises applying an organic semiconductor or a precursor thereof by spin coating.

5. (Currently amended) ~~A method as claimed in~~The method of claim 1, wherein the dielectric layer comprises an initiator sensitive for actinic radiation and functions after irradiation as a mask for the patterning of the organic semiconductor layer.

6. (Currently amended) ~~A method as claimed in~~The method of claim 45, wherein the dielectric layer comprises a photoresist material.

7. (Currently amended) ~~A method as claimed in~~The method of claim 1, comprising the additional step of providing an electro-optical layer so as to provide a display arrangement.

8. (Currently amended) ~~A method as claimed in~~The method of claim ~~6~~7 wherein the substrate is substantially transparent.

9. (Currently amended) An electronic device comprising a plurality of field effect transistor on a substrate and an interconnect structure so as to connect the transistors mutually and/or to an output terminal, the field effect transistors and at least part of the interconnect structure being provided in a stack of:

a patterned first conductor layer applied on the substrate;

an organic semiconductor layer applied on the first conductor layer;

a dielectric layer applied on the organic semiconductor layer;

a patterned second conductor layer applied on the dielectric layer;

wherein the organic semiconductor layer and the dielectric layer are provided in a substantially identical pattern.

10. (Currently amended) ~~An~~The electronic device ~~as claimed in~~of claim 9, wherein the organic semiconductor layer and the dielectric layer are absent from areas not associated with the field effect transistors and from areas not associated with crossing conductors of the first and second conductor layer.

AMENDMENTS TO THE DRAWINGS

The attached (2) sheets include changes to Figs. 1 and 5 on sheets 1 and 2 (of 4) of the original drawings.

Figure 1 has been changed to include the "Prior Art" descriptor.

Figure 5 has been modified to correspond to the written description. The reference numbers 307 and 309, and their associated lead lines have been modified to correspond to the written description (see, paragraphs 0057 and 0068 of Applicants' published application 2006/0223218).

Attachment: (2) Replacement Drawing Sheets (1 and 2 of 4)

REMARKS

Applicants have considered the Office Action dated April 17, 2007, and the references cited therein. Claims 1-10 are presently pending. No claims presently stand allowed. Applicants have made stylistic amendments to the claims, but have not modified their scope.

Applicants traverse the rejections of each and every one of the claims over the cited prior art as well as the provisional obviousness-type double patenting rejection. With regard to the obviousness-type double patenting rejection, Applicants will respond appropriately when allowable subject-matter is identified in at least one of the pending applications. With regard to the rejection of claims 1-10 as anticipated by Dimitrakopoulos et al. US 2004/0161873 A1 (Dimitrakopoulos), Applicants respectfully submit that independent claims 1 and 9 are directed to a conformal layering of patterned/structured organic semiconductor and dielectric components of a field effect transistor that is neither disclosed nor remotely suggested by the Dimitrakopoulos reference.

Applicants have amended the drawings in response to the Office Action's request for corrections.

Applicants request favorable reconsideration of the Office Action's grounds for rejecting the previously pending claims in view of Applicants' Amendments and Remarks provided herein below. Please charge any fee deficiencies to Deposit Account No. 12-1216.

Summary of the Rejections

1. Claims 1-10 are rejected as anticipated under 35 U.S.C. §102(e) in view of Dimitrakopoulos.

2. Claims 1-10 are provisionally rejected under obviousness-type double patenting.

Applicants traverse the grounds for each and every rejection for at least the reasons set forth herein below. Applicants address the specific rejections in the order they arise in the Office Action.

Applicants Traverse the 102(e) Rejection of Claims 1-10 as Anticipated by Dimitrakopoulos

Applicants have carefully considered the teachings of Dimitrakopoulos, and traverse the rejection of **claim 1** because Dimitrakopoulos neither discloses nor suggests each of the elements of Applicants' claimed method of manufacturing an electronic device. Applicants' claimed invention recites a method including a set of particular steps for building the structures making up a field effect transistor. The claimed method is illustratively depicted and described, by way of example, in FIG. 2 of Applicants' drawings and corresponding written description. See paragraphs [0048]-[0055] of Applicants' published application. Among other things, the claimed method includes a step of "patterning the organic semiconductor layer and the dielectric layer together" and wherein the dielectric layer is provided on the organic semiconductor layer which is not even remotely disclosed in Dimitrakopoulos. Applicants address the shortcomings of the teachings of the Dimitrakopoulos reference herein below.

As noted previously herein above, Dimitrakopoulos does not disclose or suggest Applicants' recited method. Applicants have duly considered the teachings of FIGs. 1a-7h and the corresponding written description of Dimitrakopoulos. Each of the figures is addressed below. FIGs. 1a-b disclose monolayer forming modules that are deposited respectively on an organic or oxide surface, and also on a metal surface. FIG. 2 depicts a thin film transistor structure, wherein the organic layer 16 is on top of a dielectric layer 14. The ordering of these layers is contrary to Applicants' recited layering in the claimed method (and electronic device recited in independent claim 9). In particular claim 1 recites: "applying a dielectric layer on the semiconductor layer". Similarly, claim 9 recites: "a dielectric layer applied on the semiconductor layer." Therefore, FIG. 2 does not disclose the invention recited in claim 1 (or claim 9). FIG. 3 of Dimitrakopoulos shows a semiconductor layer applied to a dielectric layer (the opposite of Applicants' claimed step).

Turning to FIG. 4 of Dimitrakopoulos, a dielectric layer is applied on an organic semiconductor layer. However, it is clear from FIG. 4 that the organic layer and the dielectric layer are not formed in a substantially same pattern. Instead, Dimitrakopoulos discloses a dielectric layer 14 that extends substantially beyond the organic semiconductor layer 16. Since

their patterns do not match (contrary to Applicants' claim 9), the dielectric layer 14 and organic semiconductor could not possibly be patterned together in accordance with Applicants' invention recited in claim 1.

FIGs. 5, 6 and 7 similarly do not provide any disclosure that one skilled in the art could interpret as disclosing Applicants' claimed ordering of applying the organic semiconductor and dielectric layers or the patterning of the organic semiconductor and dielectric layers together.

Dimitrakopoulos does not disclose a conformal process wherein the organic semiconductor and dielectric layers are patterned together (resulting in the two layers having a substantially same pattern). Instead, Dimitrakopoulos discloses applying a self-assembled monolayer (paragraph 14) prior to deposition of an organic semiconductor layer. Depending on the nature of the surface upon which the monolayer is applied, the material for the monolayer is selected from RZ or RZ2 in the case where the surface is an organic or dielectric surface and RSH or R(SH)2 if the surface is a metal surface. Even assuming, for sake of argument, that the layers are patterned together in a same pattern, the order in which the layers are applied in Dimitrakopoulos is the opposite of the method recited in claim 1 wherein the organic semiconductor layer is applied, and then the dielectric layer is applied. Therefore, even if the fabrication method disclosed in Dimitrakopoulos, including prior deposition of the self-assembled monolayer, causes conformance in structure with the organic semiconductor layer, conformance would be with *the layer below*, not conformance with the dielectric layer *above the organic semiconductor*. Applicants' interpretation of Dimitrakopoulos' disclosure is confirmed by the structure depicted in FIG. 4, which shows that the structure in the organic layer 16 is substantially smaller than the structure in the dielectric layer – i.e., there is clear non-conformity between the organic semiconductor layer and the dielectric layer.

For at least the above reasons, **claims 2-8** that depend from claim 1 are not anticipated by Dimitrakopoulos. Applicants' reserve their arguments regarding the individual patentability of claims 2-8 in the event that proper grounds are identified for rejecting claim 1 from which they depend.

As noted previously above with regard to Applicants' traversal of claim 1, Applicants traverse the rejection of independent **claim 9** for substantially the same reasons as those set forth herein above with regard to the rejection of claim 1 regarding the relative positions and patterning of the organic semiconductor and dielectric layers. In this regard, Dimitrakopoulos clearly does not anticipate claim 9 (see, e.g., FIG. 4 with substantially non-conforming organic semiconductor and dielectric layers). **Claim 10**, which depends from claim 9, is patentable over Dimitrakopoulos for at least the reasons set forth regarding claim 9.

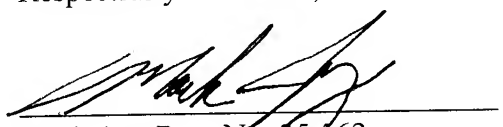
Applicants Traverse The Provisional Double Patenting Rejection of Claims 1-10

Applicants traverse the provisional obviousness-type double patenting rejection of **claims 1-10**. Since no claims have been identified as allowable in either application, such rejection is premature. Applicants will address the obviousness-type rejection when allowable subject matter is identified in either of the applications.

Conclusion

Applicants respectfully submit that the patent application is in condition for allowance. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,



Mark Joy, Reg. No. 35,562
LEYDIG, VOIT & MAYER, LTD.
Two Prudential Plaza, Suite 4900
180 North Stetson Avenue
Chicago, Illinois 60601-6731
(312) 616-5600 (telephone)
(312) 616-5700 (facsimile)

Date: August 17, 2007

Prior Art

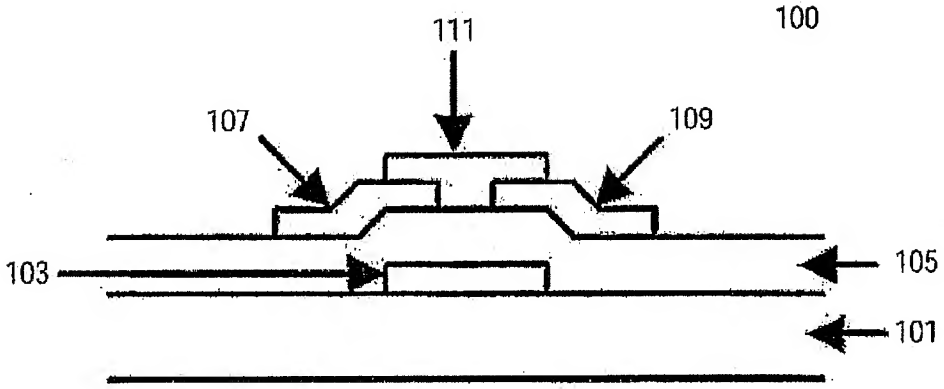


FIG.1

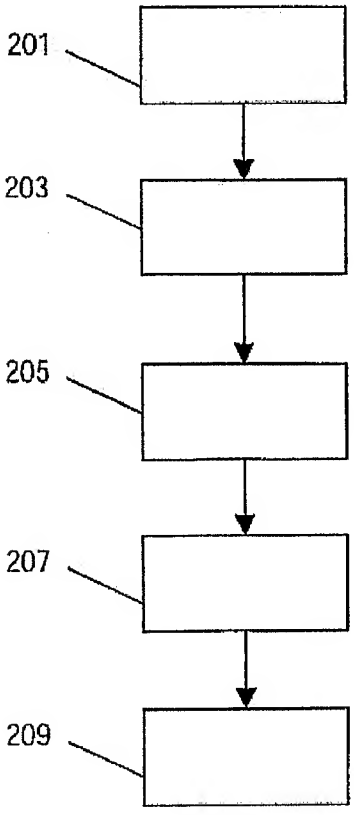


FIG.2

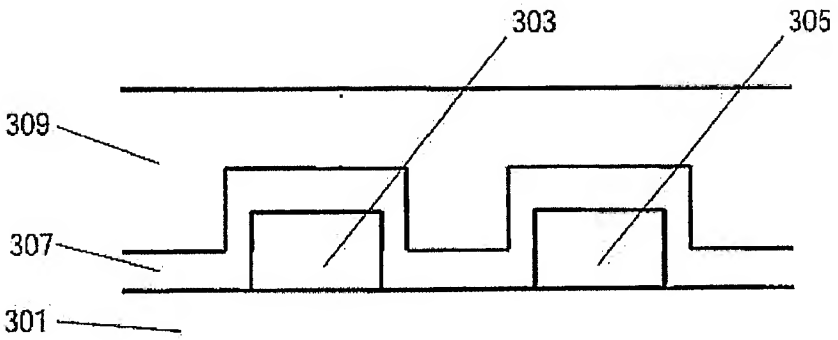


FIG.3

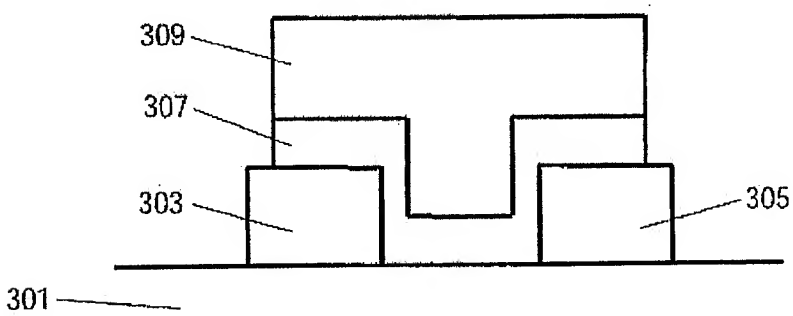


FIG.4

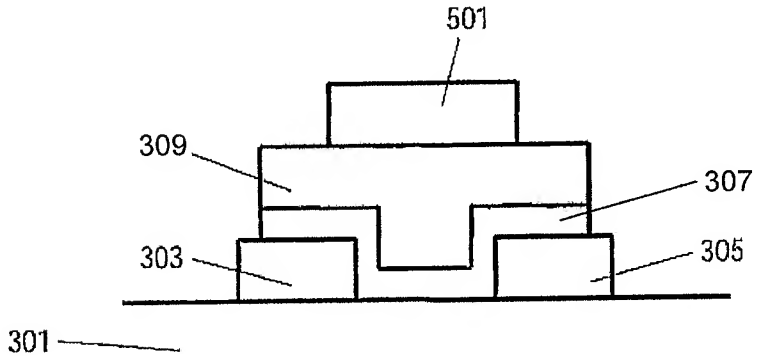


FIG.5